IN THE CLAIMS

Claim 1 (currently amended). A method of fabricating a semiconductor chip including a top passivation layer and an underlying passivation layer formed over the chip comprising the step of:

forming at least two alignment marks ~~in or on the passivation layer~~by depositing material over the underlying passivation layer, and then covering the material with the top passivation layer so that bumps are formed in the top passivation layer over the material, the bumps and material comprising the alignment marks.

Claim 2 (previously presented). The method according to claim 1 further comprising the step of selectively processing a portion of the chip using the marks to locate said portion, the processing selected from etching and adding material.

Claim 3 (currently amended). The method according to claim 1 wherein the ~~alignment marks comprise~~material comprises a metal ~~formed on a top surface of the passivation layer~~.

Claim 4 (cancelled)

Claim 5 (cancelled)

Claim 6 (previously presented). The method according to claim 1 wherein the marks are in the shape of crosses.

Claim 7 (previously presented). The method according to claim 6 wherein the marks include rectangular portions at one or more ends of the crosses, the number of portions depending upon the quadrant of the chip in which the mark is positioned.

Claim 8 (previously presented). The method according to claim 1 wherein there are at least four alignment marks, one at each corner of the chip.

Claim 9 (currently amended). A semiconductor chip comprising:

a first passivation layer as a top layer;

a second passivation layer as an underlying layer; and

at least two alignment marks ~~formed in or on the passivation layer to provide topological features for locating selected areas of the chip~~comprising material deposited over the underlying passivation layer and covered by the top passivation layer so that bumps are formed in the top passivation layer over the material.

Claim 10 (currently amended). The chip according to claim 9 wherein the ~~alignment marks comprise~~material comprises a metal ~~formed on a top surface of the passivation layer~~.

Claim 11 (cancelled)

Claim 12 (cancelled)

Claim 13 (previously presented). The chip according to claim 9 wherein the marks are in the shape of crosses.

Claim 14 (previously presented). The chip according to claim 13 wherein the marks include rectangular portions at one or more ends of the crosses, the number of portions depending upon the quadrant of the chip in which the mark is positioned.

Claim 15 (previously presented). The chip according to claim 9 wherein there are at least four alignment marks, one at each corner of the chip.

Claim 16 (new). The method according to claim 2 wherein a focused ion beam is used to locate said portion.

Claim 17 (new). The chip according to claim 9 wherein the alignment marks are adapted to permit location by a focused ion beam.